

CLAIMS

What is claimed is:

1           1.    A composite NMOS device having a source connection,  
2   a drain connection and a gate connection for conducting an  
3   operating current comprising:

4           a first NMOS device having a source, a drain and a gate;

5           a second NMOS device having a source, a drain and a  
6   gate;

7           the source of the second NMOS device being connected to  
8   the drain of the first NMOS device;

9           the gates of the first and second NMOS devices being  
10   coupled together;

11          the gate of the first NMOS device being coupled to the  
12   gate connection, the drain of the second NMOS device being  
13   coupled to the drain connection and the source of the first  
14   transistor being coupled to the source connection;

15          the second NMOS device having a lower threshold voltage  
16   than the first NMOS transistor.

1           2.    The composite NMOS device of claim 1 wherein the  
2   gates of the first and second NMOS devices are connected  
3   together, and wherein the threshold of the first NMOS device  
4   exceeds the gate - source voltage of the second NMOS device  
5   when conducting the operating current.

1           3.    The composite NMOS device of claim 2 wherein the  
2   second NMOS device is a native device.

1           4.    The composite NMOS device of claim 2 wherein the  
2   second NMOS device has a substantially zero threshold.

1           5.    The composite NMOS device of claim 1 wherein the  
2   gates of the first and second NMOS devices are coupled  
3   together through a bias control.

1           6.    The composite device of claim 5 wherein the bias  
2   control compensates for variations in temperature and  
3   processing.

1           7.    The composite NMOS device of claim 5 wherein the  
2   bias control is coupled to the gate of the second NMOS device  
3   through a resistor, and wherein the gates of the first and  
4   second NMOS devices are AC coupled together.

1           8.    A composite NMOS device having a source connection,  
2   a drain connection and a gate connection for conducting an  
3   operating current comprising:

4           a first NMOS device having a source, a drain and a gate;

5           a second NMOS device having a source, a drain and a  
6   gate;

7 the source of the second NMOS device being connected to  
8 the drain of the first NMOS device;

9 the gate of the second NMOS device being coupled to the  
10 source of the first NMOS device;

11 the gate of the first NMOS device being coupled to the  
12 gate connection, the drain of the second NMOS device being  
13 coupled to the drain connection and the source of the first  
14 transistor being coupled to the source connection;

15 the second NMOS device having a lower threshold voltage  
16 than the first NMOS transistor.

1 9. The composite NMOS device of claim 8 wherein the  
2 second NMOS device is a native device.

1 10. The composite NMOS device of claim 8 wherein the  
2 second NMOS device has a substantially zero threshold.

1 11. The composite NMOS device of claim 8 wherein the  
2 gate of the second NMOS device is coupled to the source of  
3 the first NMOS device through a bias control.

1 12. The composite NMOS device of claim 11 wherein the  
2 bias control compensates for variations in temperature and  
3 processing.

1 13. The composite NMOS device of claim 12 wherein the  
2 bias control is coupled to the gate of the second NMOS device

3 through a resistor, and wherein the gates of the first and  
4 second NMOS devices are AC coupled.

1 14. A source follower for conducting an operating  
2 current, the source follower having a positive power supply  
3 connection, a circuit ground connection, a source follower  
4 input connection and a source follower output connection  
5 comprising:  
6 a first NMOS device having a source, a drain and a gate;  
7 a second NMOS device having a source, a drain and a  
8 gate; and  
9 a current source;  
10 the source of the second NMOS device being connected to  
11 the drain of the first NMOS device;  
12 the gates of the first and second NMOS devices being  
13 coupled together;  
14 the gate of the first NMOS device being coupled to the  
15 source follower input connection, the drain of the second  
16 NMOS device being coupled to the positive power supply  
17 connection and the source of the first transistor being  
18 coupled to the source follower output connection and through  
19 the current source to the circuit ground connection;  
20 the second NMOS device having a lower threshold voltage  
21 than the first NMOS transistor.

1           15. The source follower of claim 14 wherein the gates  
2 of the first and second NMOS devices are connected, and  
3 wherein the threshold of the first NMOS device exceeds the  
4 gate - source voltage of the second NMOS device when  
5 conducting the operating current.

1           16. The source follower device of claim 15 wherein the  
2 second NMOS device is a native device.

1           17. The source follower device of claim 15 wherein the  
2 second NMOS device has a substantially zero threshold.

1           18. The source follower device of claim 14 wherein the  
2 gates of the first and second NMOS devices are coupled  
3 through a bias control.

1           19. The source follower of claim 18 wherein the bias  
2 control compensates for variations in temperature and  
3 processing.

1           20. The source follower of claim 18 wherein the bias  
2 control is coupled to the gate of the second NMOS device  
3 through a resistor, and wherein the gates of the first and  
4 second NMOS devices are AC coupled.

1           21. A source follower for conducting an operating  
2 current, the source follower having a positive power supply  
3 connection, a circuit ground connection, a source follower  
4 input connection and a source follower output connection  
5 comprising:

6           a first NMOS device having a source, a drain and a gate;  
7           a second NMOS device having a source, a drain and a  
8 gate; and

9           a current source;

10          the source of the second NMOS device being connected to  
11 the drain of the first NMOS device;

12          the gate of the second NMOS device being coupled to the  
13 source of the first NMOS device;

14          the gate of the first NMOS device being coupled to the  
15 source follower input connection, the drain of the second  
16 NMOS device being coupled to the positive power supply  
17 connection and the source of the first transistor being  
18 coupled to the source follower output connection and through  
19 the current source to the circuit ground connection;

20          the second NMOS device having a lower threshold voltage  
21 than the first NMOS transistor.

1           22. The source follower of claim 21 wherein the second  
2 NMOS device is a native device.

1           23. The source follower of claim 21 wherein the second  
2 NMOS device has a substantially zero threshold.

1           24. The source follower claim 21 wherein the gate of  
2 the second NMOS device is coupled to the source of the first  
3 NMOS device through a bias control.

1           25. The source follower of claim 24 wherein the bias  
2 control compensates for variations in temperature and  
3 processing.

1           26. The source follower of claim 25 wherein the bias  
2 control is coupled to the gate of the second NMOS device  
3 through a resistor, and wherein the gates of the first and  
4 second NMOS devices are AC coupled.